REMARKS

This is in response to the Official Action currently outstanding in the above-identified application.

Claims 1-34 were originally presented. Claims 1-25 were elected for further prosecution and Claims 26-34 were cancelled, without prejudice. Claims 35 – 45 were added by a previous Amendment. The next previous Amendment amended Claims 2 and 9, and canceled Claims 4 and 7. The present Amendment amends Claim 23 to correct an inadvertent error in the restatement thereof in the next previous Amendment, but otherwise does not propose any further amendments, deletions or additions of any claims. Accordingly, upon the entry of the foregoing Amendment, the claims under active prosecution in this application will be Claims 1 – 3, 5 – 6, 8 - 25 and 35 – 45.

The claims as they will stand upon the entry of the foregoing Amendment are set forth in full hereinabove as required by the Rules.

In the currently outstanding Official Action, the Examiner has:

1. Failed to acknowledge Applicants' claim of foreign priority under 35 USC 119(a)-(d), or to confirmed the safe receipt of the priority document for this application by the United States Patent and Trademark Office; however, Applicants note that the Examiner previously acknowledged these documents in this prosecution.

2. Acknowledged that as a result of an appropriately filed Request for Continued Examination the finality of the previous Official Action has been withdrawn, indicated that Applicants' submission of 30 October 2003 has been entered, and indicated that the currently outstanding Official Action is non-final;

3. Indicated that Claims 1, 5, 8-10, 12, 14, 16, 18, 20, 22, 24 and 35-45 are allowed;

4. Rejected Claims 2-3, 6, 11, 13, 15, 17, 19, 21, 23 and 25 under 35 USC 112, first paragraph, as failing to comply with the written description requirement in that the rejected claims contain subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors at the time that the application was filed had possession of the claimed invention;

5. Objected to the drawings as failing to show the features specified in the claims that form the basis of his rejection under 35 USC 112, and required correction;

6. Objected to Claims 23 and 25 on the basis that in the next previous amendment Applicants misstated the dependency of Claim 23 as being from Claim 20, rather than from Claim 21, and required correction;

7. Rejected Claim 2 under 35 USC 103(a) as being unpatentable over the Cairns, et al. reference (U.S. Patent No. 6,266,041);

8. Rejected Claims 3, 6, 11, 13, 15, 17, 19 and 21 under 35 USC 103(a) as being unpatentable over the Cairns, et al. reference in view of the Ogawa reference (U.S. Patent 6,018,331);

9. Rejected Claims 23 and 25 under 35 USC 103(a) as being unpatentable over the Cairns, et al. reference in view of the Ogawa reference, and the Ino, et al reference (U.S. Patent 5,903,014); and

10. Provided Applicants with a Statement of his Response to Applicants' previous arguments wherein he indicates that Applicants' previous arguments have been considered but are not deemed to be persuasive in view of the 35 USC 112 rejection referred to in item 4 above, and that in view of that 35 USC 112 rejection he has examined this case based upon his "best understanding of the claim language".

With regard to items 1 – 3, further detailed discussion in these Remarks is not believed to be necessary.

With respect to items 4, 5 and 9, the Examiner has asserted that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claimed invention, i.e., the original disclosure, when filed, did not contain a disclosure supporting "at least one of the switching circuits electrically disconnects at least one of the latch circuits from the clock signal line...in response to cyclic signals separate from control signals". Further, the Examiner has asserted that that same subject matter is not shown in the drawings as filed, and that the drawings must be amended to include that subject matter without the addition of so-called "new matter" to the application, or the subject matter in question must be removed from the claims.

In addition, the Examiner appears to have effectively indicated that he has not considered the claims as including the alleged "new matter" (i.e., "at least one of the switching circuits electrically disconnects at least one of the latch circuits from the clock signal line...in response to cyclic signals separate from control signals") in the course of rendering the currently outstanding substantive rejections. In this regard, attention is respectfully directed to page 3, lines 3-4 and page 9, section 10 of the currently outstanding Official Action.

Applicants do not agree with the Examiner's position in the foregoing regards and consequently respectfully **traverse** the outstanding rejections based thereon. In support of this traversal, the Applicants have the following comments.

The Examiner admits that at page 33, lines 10-15 and at page 37, lines 10-18, the present specification discloses "the reset RST is supplied to the latch circuits in synchronization with the pulse PLS supplied cyclically at regular intervals", but asserts that this is not enough to support the wording added to the claims by the Amendment Accompanying Request for Continued Examination (which also according to the Examiner is not presently shown in the drawings).

The Examiner also admits that the disclosure in the specification as filed and the drawings as filed are sufficient to support the claimed circuit initiation structure and operation (see allowed Claim 1 and the specification at page 11, line 22 to page 12, line 12). However, Applicants respectfully submit that the Examiner has failed to note that the specification is more detailed than the Summary of the Invention portion thereof in that it further states at page 27, lines 6-25, that:

> Fig. 1 shows a shift register circuit 1 according to an embodiment of the invention.
> The shift register circuit 1 is made up of a plurality of latch circuits LATA, LATB having the arrangement shown in Figs. 26 and 27, a plurality of logical OR circuits OR, and a plurality of switches ASW. The foremost latch circuit of the shift register circuit 1 shown in Fig. 1 may be either a latch circuit LATA or a latch circuit LATB, and this is determined depending on an input clock signal.

> It is controlled by the logical OR circuits OR and the switches ASW whether or not clock signals CLK,/CLK are input to the latch circuits LATA, LATB. For example, a logical OR circuit OR belonging to one unit 2 receives a signal output from a latch circuit of a preceding stage to a latch circuit belonging to the one unit 2 ***as well as a signal output from the latch circuit belonging to the unit 2***, and then computes a logical OR of those signals. ***Based on a signal which indicates a result of computation, a switch ASW belonging to the one unit 2 goes conducting, or closed, so that clock signals CLK, /CLK are supplied to the latch circuit belonging to the one unit 2.*** *(Emphasis added)*

Further, the specification states at page 32, line 23 to page 33, line 14, that:

> Figs. 8 and 9 show other examples of the latch circuits of the shift register 1 as LATA1 and LATB1.
> In the latch circuits LATA1, LATB1, the internal nodes are forcedly reset. As a result of the reset, for example, signals output from the latch circuits go low level.
> Figs. 10B, 10C and Figs. 11B, 11C show clock signals CLK and reset signals RST for the latch circuits LATA1, LATB1.
> In the example of the signal waveform shown in Figs. 10A-10C, the reset signal RST is supplied to the latch circuits LATA1, LATB1 only when power is turned on, ***whereby internal nodes of those latch circuits are initialized***.
> In the example of the signal waveform shown in Figs. 11A-11C, ***the reset signal RST is supplied to the latch circuits LATA1, LATB1 in synchronization with the pulse PLS supplied cyclically at regular intervals, whereby the internal nodes of those latch circuits are initialized***.
> *(Emphasis added)*

Therefore, it is Applicants' position that the facts of the present specification's content are contrary to the Examiner's stated rejection under 35 USC 112, his related drawing objections, and his effective refusal to consider the wording added by the previous amendment. Specifically, the shift register circuit is shown in Figure 1; latch circuits LATA and LATB are shown in Figures 26 and 27; latch circuits LATA1 and LATB1 are shown in Figures 8 and 9; Figures 10A-10C show the use of the reset signal in the context of "initializing" at power-on; and Figures 11A-11C show the use of the reset signals in synchronization with the regularly applied pulse PLS signals to "initialize" the internal nodes of the latch circuits to which they are applied.

Accordingly, the specification specifically recognizes (and the drawings show) that upon power on at least one of the switching circuits electrically disconnects at least one corresponding latch circuit from the clock signal line. Further, the specification goes on to explain (and the drawings to show) that "(i)t is controlled by the logical OR circuits OR and the switches ASW whether or not clock signals CLK,/CLK are input to the latch circuits LATA, LATB."

In addition, the specification specifically teaches (i) that the internal nodes of the latch circuits shown in Figures 8 and 9 are forcedly reset by the reset signal RST supplied to the latch circuits in synchronization with the pulse PLS signals, and (ii) that the opening or closing of the switch ASW depends upon a logical comparison of the states of the latch circuit and its preceding latch circuit. Effectively this is a teaching that when the nodes of a latch circuit are forcedly reset, the latch circuit assumes a state such that the logical OR circuit OR opens the switch ASW so as to disconnect the latch circuit from the clock signal. According to the specification this occurs both at power on (see Figures 10A-10C) and at reset (see Figures 11A-11C).

The exact words of the claim are not required to appear in the specification in order to provide the requisite support for the subject matter of the claims. What is required is a teaching of the invention in the specification that is adequate to show (disclose to one of ordinary skill in the art) that the inventors were in possession of the invention at the time the application was filed. Based upon the foregoing analysis, Applicants respectfully submit that such is the case in this application.

Accordingly, Applicants respectfully submit that one skilled in the art knowing that the state of the latch circuit is a determining factor as to whether or not the latch circuit is to be connected or disconnected from the clock would certainly know that the reset of the nodes of the latch circuit would place it in a condition such that the OR logic would turn the switch ASW off. This is particularly the case in view of the fact that the specification equates the operation of the latch circuit at power on (i.e., "initialization") with the operation of the circuit at reset in the portion quoted above from pages 32 and 33.

In view of the foregoing, Applicants submit that the Examiner's objections to the drawings and his claim rejections under 35 USC 112, first paragraph, both are misplaced in the context of this application, and that those rejections and the related requirements for drawing changes should be withdrawn in response to this communication.

With respect to item 6, Applicants by the foregoing Amendment have corrected their inadvertent misstatement of the dependency of Claim 23 (from which Claim 25 depends) as being from Claim 21, rather than from Claim 20. A decision granting entry to this amendment of Claim 23 in response to this communication is respectfully requested.

With respect to items 7 through 9 above, Applicants also respectfully **traverse** the Examiner's rejections of Claims 2, 3, 6, 11, 13, 15, 17, 19 and 21, and again request reconsideration based upon the amended wording of Claim 2 in light of the foregoing discussion concerning the inappropriate nature of the Examiner's currently outstanding rejections under 35 USC 112, first paragraph. Applicants' substantive bases for this traversal and request for reconsideration are two-fold and as asserted in the next previous Amendment. Those bases are restated below for the convenience of the Examiner.

First, in response to the Examiner's observation that claim 2 did not specifically recite the initialization of the shift register at power-on as well as at regular intervals thereafter in substantially the same manner as at power-on, Applicants previously amended Claim 2 so as to specifically include those features. Applicants respectfully submit that no new matter was introduced by that amendment. This view is supported by the facts (i) that the disconnection of at least one of the latch circuits at regular intervals separately controlled from the normal switching of the latch circuits was previously contemplated by the language of the claim and (ii) that the specification clearly indicates that the initialization that takes place due to such a disconnection (reset) of a latch circuit causes the same initialization sequence as power-on (see discussion of rejection under 35 USC 112, first paragraph above).

Second, a key element to the support necessary to establish a *prima facie* case of obviousness is that there must be a suggestion contained within the prior art relied upon to make the combination with the features of the invention. In other words, the Examiner must establish ***why*** a person of ordinary skill in the art at the time the invention was made would have been motivated by that art to make the invention at issue.

In particular, in cases such as this wherein the reference does not expressly or impliedly suggest the claimed invention, the Examiner has an obligation to present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. See, *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985); *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed Cir. 1999); *McGinley v. Franklin Sports Inc.*, 262 F. 3d 1339, 60 USPQ2d 1001 (Fed Cir. 2001)); *In re Sang Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Feb Cir. 2002); *In re Huston*, (Slip Op. 02-1048 (Fed Cir. October 2002))

Applicants respectfully submit that the Examiner in the present circumstances has failed to provide such a convincing line of reasoning. Consequently, it is respectfully submitted that the Examiner has failed in his burden of establishing a *prima facie* case in support of his rejections under 35 USC 103, and that the currently outstanding rejections should be found to be insufficient and withdrawn in response to this communication.

In particular, the Examiner has not established any basis for his assertion that the circuit shown in Fig. 3 of the Cairns reference operates in the manner that he attributes to it. Instead, it is to be recognized that the Cairns reference simply (i) states that: "...it is known to apply state controlled clocking schemes to the shift register" (see Cairns, Col. 2, lines 31-32), and (ii) claims that the programmed shift elements of the shift register contain more than one occurrence of each logic state (see, Cairns Claim 1).

Thus, there is no specific teaching, disclosure or suggestion in the Cairns reference, of which Applicants are presently aware, to the effect that "the left most switching circuit 23 electrically disconnects the left most plurality of DDF circuits from the clock signal ***at regular intervals*** determined by the output of the left most OR gate 22 as shown in Fig. 3" (emphasis added) as the Examiner suggests in the currently outstanding rejection.

In fact, quite the opposite of the foregoing appears to be the case in view of the Examiner's own characterization that "Cairns discloses the signals HSYNC is vary *(i.e., are to vary)* in accordance with the pulse signal transferred and a plurality of switching circuits 23 each connect and disconnect corresponding to the latch circuit to/from the clock signal line CL". Thus, while the Cairns reference may disclose a variable operation of the switching circuits that transfer a pulse signal sequentially along the shift register, there is no disclosure in the Cairns reference that at least one of the switching circuits disconnects at least one of the latch circuits from the clock signal line ***at power on and at regular intervals*** thereafter in response to cyclic signals separate from the control signals that control the normal operational switching of the connections of the latch circuits to the clock as the pulse travels along the shift register as now specifically claimed in the present application.

Accordingly, the Examiner's rejection is respectfully submitted to be insufficient to establish a *prima facie* case supporting his conclusion of the obviousness of the rejected claims of this application. In view of the foregoing amendment and argument, reconsideration of the Examiner's outstanding rejections under 35 USC 103(a) in response to this submission is respectfully requested.

For each, and all, of the foregoing reasons, Applicants respectfully submit that the Examiner's currently outstanding rejections are in error, and that Claims 1 – 3, 5 –6, 8 – 25 and 35-45 of this application as now presented are in condition for allowance. Consequently, entry of the foregoing Amendment, reconsideration, and allowance of this application in response to this communication all are respectfully requested.

Applicants also believe that additional fees beyond those submitted herewith are not required in connection with the consideration of this response to the currently outstanding Official Action. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge and/or credit Deposit Account No. **04-1105**, as necessary, for the correct payment of all fees which may be due in connection with the filing and consideration of this communication.

Respectfully submitted,

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